Sigma-Delta Converters and the V200

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Document Revision: 1.2
Document Date: August 6, 1997

1. Introduction

The purpose of this document is to acquaint the user with sigma-delta ADC technology, its advantages, and how it is implemented in the V200.

The sigma-delta ADC can be thought of as a very high sampling rate ADC with very poor (1-bit) resolution. The bitstream from the ADC is then *averaged and down-sampled* to achieve improved resolution at a lower *effective* sampling rate. The *averaging* is accomplished with a Finite Impulse Response (FIR) digital filter.

Recent advances in high speed digital electronics has made the sigma-delta ADC architecture competitive with more traditional ADC architectures.

Radical differences in sigma-delta over conventional ADC technology requires re-thinking a number of technical considerations. These include:

Gain vs Input Span The term *gain* has meaning when it is understood that the input to the ADC is ±10 Volts. With sigma-delta ADCs the input to the ADC is typically not ±10 Volts so the relevant parameter is *input span* instead of *gain*.

Oversampling and Antialias Filtering In conventional ADCs it is frequently necessary to sample at the lowest feasible rate to bound system throughput. When signal aliasing is of concern very sharp low-pass analog filters are typically required. The closer the Nyquist frequency (sampling-rate/2) is to the upper end of the passband the sharper the filter requirement. The high (64:1) oversampling rate of the sigma-delta greatly reduces the need for sharp analog

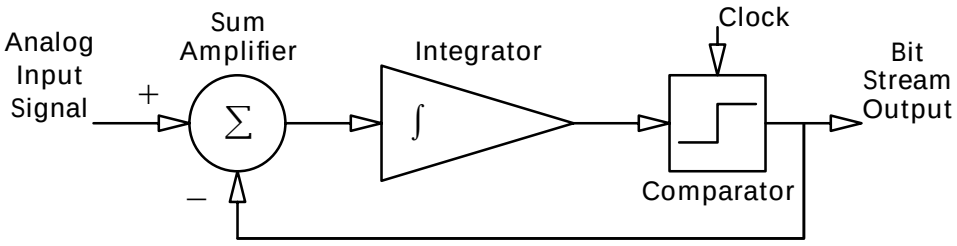

Figure 1: Typical Sigma-Delta Architecture

filters. Digital filtering and decimation internal to the sigma-delta minimize system throughput requirements for a given system bandwidth requirement.

"Simultaneous" Sampling In conventional multiplexed or ADC per channel configurations *simultaneous sampling* (sample and hold per channel) is required when relative phase or samples between different channels is to be compared. The oversampling and "digital averaging" of the sigma-delta presents unique differences in the concept of *simultaneous sampling.*

2. Sigma-Delta Operation

The typical sigma-delta ADC is illustrated in Figure 1. The analog input signal and a bitstream whose bit density of 1's bits is a representation of the magnitude of the analog signal are fed into a summing amplifier. This is then integrated and enters a comparator which outputs a 0 or 1 depending whether the output of the integrator is below or above the comparators threshold.

The simplest way to understand the operation is to assume a slight variation from a steady state condition and trace what happens. For example, assuming a positive analog input, if the *average* 1's bitstream density at the negative input of the summing amplifier is high compared to the analog input, then the output of the summing amplifier will be negative. This over time results in a corresponding drop in integrator output and the comparator output generating 0's. The 0's in turn cause increased positive output of the summing amplifier which over time results in higher integrator output, and 1's at the comparator output.

It should be clear from the above discussion that the *average* density of the bitstream must closely track the analog input signal. Any deviation will quickly result in the average bitstream density from the comparator being adjusted to follow the analog input signal. The comparator is in effect a very high gain amplifier whose

output is driven to “1” or “0” very quickly depending on the difference between the input and the reference.

This action forms a strong, high gain, negative feedback loop which gives the sigma-delta ADC excellent linearity and no missing codes. It also minimizes the effects of component drift with time making the sigma-delta very stable compared with its “open loop cousins.”

3. Oversampling, Averaging, and Resolution

The sigma-delta modulator discussed above is essentially an ADC with one bit resolution. Resolution can be increased by averaging. Thus by averaging the output of the sigma-delta modulator the resolution of the analog signal level can be improved. A low-pass digital filter is a form of averaging. In fact an N-point average is no more than an N-tap Finite Impulse Response (FIR) digital filter with coefficients of 1/N.

In the Analog Devices AD-7722, which is the sigma-delta ADC that is used in the V200, there are two FIR filters. The first is a 384 tap filter that samples the output of the sigma-delta modulator at the clock frequency f_{clkin} followed by a second 151 tap filter that samples the output of the first filter at $f_{clkin}/32$ and decimates the output by a factor of two. In effect the second filter averages over $151 \times 32 = 4832$ analog samples to achieve 16-bits of resolution and the *effective* sample rate is $f_{clkin}/64$.

3.1. Antialias Filtering

The V200 includes a 2-pole RC antialias filter and a two stage digital FIR decimating filter. The high 64:1 oversampling ratio of the sigma-delta ADC pushes the first band of frequencies aliased into the 0 — 92 KHz passband out to the 12.8 MHz region when the V200 is operated at a maximum effective sample rate of 200 Ksamples/second (f_{clkin} = 12.8 MHz). Refer to Figure 2.

The 2-pole RC antialias filter ahead of the sigma-delta provides >54dB of attenuation in the 12.8 MHz region. This is adequate for most applications since it rare for the signal source to have significant frequency components at 64 times the upper end of the frequency region of interest (passband). The digital filters provide high attenuation (>90 dB) for signals in the stopband above 106.34 KHz. This includes aliased signals which fall within the stopband. Furthermore the FIR digital filters provide excellent channel to channel matching and linear phase response.

This contrasts with a conventional ADC where sampling rate and throughput limitations force minimum sampling rates and thus the Nyquist frequency to be as

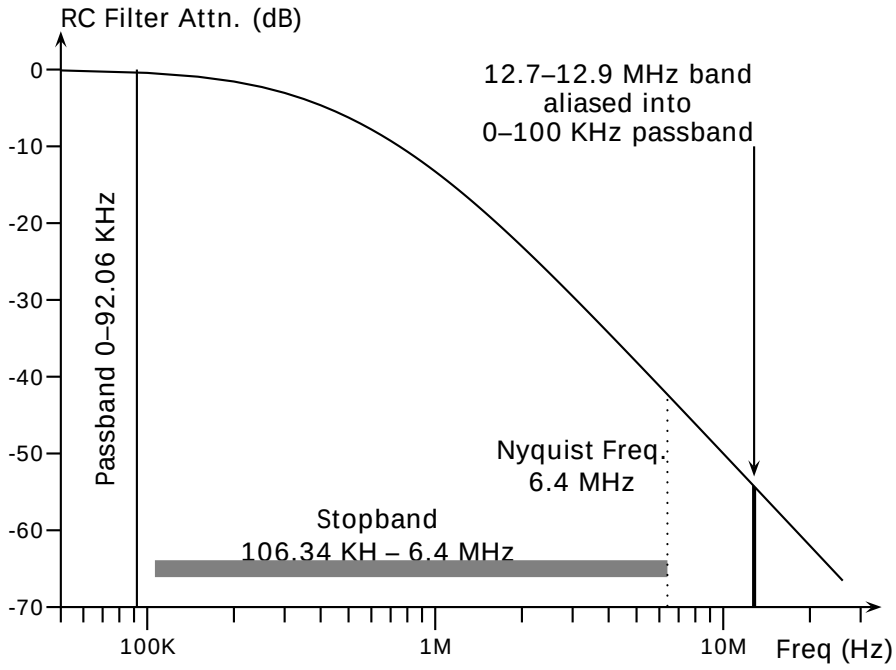

Figure 2: V200 2-Pole RC Antialias Filter Characteristics

close to the upper passband edge as possible. Since some transducers can have significant signal power above the region of interest, lowpass filters with much higher attenuation at the lower aliased frequencies are frequently required.

The decimating FIR digital filter in the sigma-delta ADC provides a very sharp cutoff above 92 KHz passband, and >90dB attenuation in the stopband above 106.34 KHz when operated at an effective sample rate of 200 samples/sec.

As a result of the high oversampling rate of the sigma-delta, a simple two pole RC filter provides excellent antialias protection in most cases. Several factors contribute. The high oversampling rate pushes the band of frequencies aliased into the passband out to high frequencies where the RC filter has good attenuation (refer to Figure 2. Also at this higher frequency the original signal is likely to have significantly smaller frequency components. Finally the digital filter which is part of the sigma-delta highly attenuates signals above the stopband edge.

4. "Simultaneous Sampling" with Sigma-Delta ADCs

Due to the architecture of the sigma-delta ADC which uses digital filtering and decimation techniques, the concept of *simultaneous sampling* loses its literal meaning since any given output sample is a weighted average over some number of input samples. Thus there is no well defined *time* when the analog signal was "sampled." This, however **does not** preclude the output of two different channels being time or phase related.

Running sigma-delta ADCs from a common clock is sufficient to guarantee a fixed phase relationship between the channels. By also resetting the ADCs from a common reset signal the absolute phase difference between channels can be eliminated.

In most applications the *real requirement* is either a stable or zero phase relationship between different channels **not simultaneous sampling.** Simultaneous sampling is only *one* means to an end that works for conventional ADCs. Obviously sigma-delta ADCs *can meet* the *real* requirement.

In a few applications there is a need to establish a "true" zero time relative to some event. For example the firing of a laser or other event. With conventional ADCs one approach is to correlate the "sample" signal with the external event to establish t=0. With sigma-delta ADCs this is not usually feasible. An alternative approach which works with sigma-delta as well as conventional ADCs is to dedicate one analog channel to sampling the trigger signal. This is probably the most accurate approach for either type of ADC.